CLAIMS

1. A clock generator circuit for providing a plurality of clock signals that have predetermined phases relative to a master clock signal, comprising:

a first locked loop comprising:

a first signal generator producing a reference clock signal at an output terminal, the reference clock signal having a phase relative to the master clock signal that is a function of a first control signal applied to a first control terminal, and

a first phase detector having a first input terminal coupled to the master clock signal, a second input terminal coupled to the reference clock signal, and an output terminal coupled to the first control terminal of the first signal generator, the first phase detector generating the control signal as function of the difference in phase between the master clock signal and the reference clock signal at the first and second input terminals, respectively; and

a second locked loop comprising:

a second signal generator coupled to the reference clock signal from the first signal generator and producing the plurality of clock signals, the phase of the clock signals relative to the reference clock signal being a function of a second control signal applied to a second control terminal, and

a second phase detector having a first input terminal coupled to the reference clock signal from the first signal generator, a second input terminal coupled to one of the plurality of clock signals, and an output terminal coupled to the second control terminal of the second signal generator, the second phase detector generating the control signal as function of the difference in phase between the reference clock signal and the clock signal applied to the first and second input terminals, respectively.

2. The clock generator circuit of claim 1 wherein the first and second locked loops comprise delay locked loops in which the first signal generator comprises a first voltage controlled delay circuit in which the master clock signal is delayed by a period determined by the first control signal to produce the reference clock signal, and the second signal generator comprises a second voltage controlled delay circuit in which the reference clock signal is delayed by a plurality of periods determined by the second control signal to produce the plurality of clock signals.

3. The clock generator circuit of claim 2 wherein the first phase detector is coupled to the output terminal of the first voltage controlled delay circuit through the second voltage controlled delay circuit so that the second input terminal of the first phase detector receives as the reference clock signal one of the plurality of clock signals from the second voltage controlled delay circuit.

4. The clock generator circuit of claim 2 wherein the second phase detector receives the reference clock signal through the second voltage controlled delay circuit so that the second input terminal of the first phase detector receives as the reference clock signal one of the plurality of clock signals from the second voltage controlled delay circuit.

5. The clock generator circuit of claim 2 wherein the first and second phase detectors are coupled to the reference clock signal through the second voltage controlled delay circuit so that the reference clock signal is coupled to the second input terminal of the first phase detector as one of the clock signals from the second voltage controlled delay circuit and the reference clock signal is coupled to the first input terminal of the second phase detector as one of the clock signals from the second voltage controlled delay circuit.

6. The clock generator circuit of claim 5 wherein the same one of the plurality of clock signals is coupled to both the second input terminal of the first phase detector and the first input terminal of the second phase detector.

7. The clock generator circuit of claim 2 wherein each of the first and second phase detectors comprise:

a phase comparator generating an enable signal during the period that the phase of the signal applied to one of its input terminals lags the phase of the signal applied to the other of its input terminals; and

a charge pump receiving the enable signal from the phase comparator, the charge pump generating as the respective first and second control signal a voltage that increases toward one polarity responsive to the enable signal and toward the opposite polarity responsive to the absence of the enable signal.

8. The clock generator circuit of claim 1 wherein the second signal generator produces N clock signals, and wherein the phase of each of the clock signals relative to the phase of the master clock signal is [M/N]*180 degrees, where M=0, 1, . . N.

9. The clock generator circuit of claim 1, further comprising a multiplexer coupled to the second signal generator to receive the plurality of clock signals and couple one of the clock signals to a clock output terminal.

10. A clock generator circuit for providing a sequence of clock signals that have predetermined phases relative to a master clock signal, comprising:

a first voltage controlled delay circuit receiving the master clock signal and generating a reference clock signal having a delay relative to the master clock signal that is a function of a first control signal;

a second voltage controlled delay circuit receiving the reference clock signal and generating the sequence of clock signals each of which has a delay relative to an adjacent clock signal in the sequence that is a function of a second control signal;

a first phase detector comparing the phase of the master clock signal to the phase of a first one of the plurality of clock signals and generating the first control signal as a function of the difference therebetween, the first voltage controlled delay circuit and first phase detector delay locking the phase of the first clock signal to the phase of the master clock signal; and

a second phase detector comparing the phase of two of the plurality of clock signals and generating the second control signal as a function of the difference therebetween, the second voltage controlled delay circuit and the second phase detector delay locking the phases of the two clock signals to each other.

11. The clock generator circuit of claim 10 wherein the first voltage controlled delay circuit and first phase detector delay lock the phase of the first clock signal to substantially the same phase as the master clock signal.

12. The clock generator circuit of claim 10 wherein the second phase detector compares the phase of the first clock signal to the phase of a last clock signal in the sequence of clock signals, and wherein the second voltage controlled delay circuit and the second phase detector delay lock the first clock signal to the inverse of the last clock signal.

13. The clock generator circuit of claim 12 wherein the clock signals in the sequence between the first and last clock signal are equally phased apart from each other and the first and last clock signals.

14. The clock generator circuit of claim 10 wherein each of the first and second phase detectors comprise:

a phase comparator generating an enable signal during the period that the phase of the signal applied to one of its input terminals lags the phase of the signal applied to the other of its input terminals; and

a charge pump receiving the enable signal from the phase comparator, the charge pump generating as the respective first and second control signal a voltage that increases toward one polarity responsive to the enable signal and toward the opposite polarity responsive to the absence of the enable signal.

15. The clock generator circuit of claim 10, further comprising a multiplexer coupled to the second voltage controlled delay circuit to receive the clock signals and couple one of the clock signals to a clock output terminal.

16. The clock generator circuit of claim 15, further comprising a multiplexer compensation circuit coupling the first clock signal from the second voltage controlled delay circuit to the phase detector after a delay corresponding to the delay that the clock signal is coupled to the clock output terminal of the multiplexer.

17. A clock generator circuit for providing a sequence of clock signals that have respective phases relative to a master clock signal, comprising:

a first delay-lock loop generating the sequence of clock signals which are increasingly delayed from a first clock signal to a last clock signal, two of the clock signals in the sequence being delay locked to each other so that they have a predetermined phase with respect to each other; and

a second delay-lock loop delay locking one of the clock signals to the master clock signal so that the clock signals in the sequence have respective phases with respect to the master clock signal.

18. The clock generator circuit of claim 17 wherein the first delay-lock loop delay locks the first clock signal and the last clock signal to each other so

that the first clock signal and the last clock signal have a predetermined phase with respect to each other.

19. The clock generator circuit of claim 18 wherein the first clock signal and the last clock signal are delay locked to each other so that they are the inverse of each other.

20. The clock generator circuit of claim 17 wherein the clock signals in the sequence are increasingly delayed in equal increments from the first clock signal to the last clock signal so that adjacent clock signals in the sequence have respective phases that are equally spaced from each other.

21. The clock generator circuit of claim 17 wherein the first delay lock loop delay locks the first clock signal and the last clock signal so that they are the inverse of each other whereby the first and last clock signals have respective phases that are 180 degrees from each other.

22. The clock generator circuit of claim 17 wherein the second delay-lock loop delay locks the first clock signals to the master clock signal so that they have substantially the same phase.

23. The clock generator circuit of claim 17 wherein the first delay-locked loop comprises:

a first voltage controlled delay circuit receiving a reference clock signal and generating the sequence of clock signals from the reference clock signal by delaying the reference clock signal by respective delays that are a function of a first control signal;

a first phase detector comparing the phase of two of the clock signals in the sequence and generating the first control signal as a function of the difference therebetween; and

wherein the second delay-locked loop comprises:

a second voltage controlled delay circuit receiving the master clock signal and generating a reference clock signal having a delay relative to the master clock signal that is a function of a second control signal; and

a second phase detector comparing the phase of the master clock signal to the phase of one of the clock signals in the sequence and generating the second control signal as a function of the difference therebetween.

24. The clock generator circuit of claim 23 wherein each of the first and second phase detectors comprise:

a phase comparator generating a first signal during the period that the phase of the signal applied to one of its input terminals lags the phase of the signal applied to the other of its input terminals and generating a second signal during the period that the phase of the signal applied to the one input terminal leads the phase of the signal applied to the other input terminal; and

a charge pump receiving the first and second signals from the phase comparator, the charge pump generating as the respective first and second control signal a voltage that increases toward one polarity responsive to the first signal and toward the opposite polarity responsive to the second signal.

25. The clock generator circuit of claim 17, further comprising a multiplexer coupled to the first delay-lock loop to receive the clock signals and couple one of the clock signals to a clock output terminal.

26. A command data latch circuit for storing a command data packet at a time determined from a command clock signal, the command data latch comprising:

a latch circuit having a data input and a clock input, the data input being adapted to receive the command data packet and store the command data packet responsive to a clock signal applied to the clock input; and

a clock generator circuit for generating the latch signal from a periodic master clock signal, the clock generator circuit comprising:

a first delay-lock loop generating the sequence of clock signals which are increasingly delayed from a first clock signal to a last clock signal, two of the clock signals in the sequence being delay locked to each other so that they have a predetermined phase with respect to each other; and

a second delay-lock loop delay locking one of the clock signals to the master clock signal so that the clock signals in the sequence have respective phases with respect to the master clock signal.

a multiplexer coupled to the first delay-lock loop to receive the clock signals and couple one of the clock signals to the clock input of the latch circuit, the clock signal coupled to the latch circuit being selected by the multiplexer as a function of a select signal applied to a control input of the multiplexer; and

a select circuit determining which of the clock signals from the first delay-lock loop should be used to cause the latch circuit to store the command data packet and generating the select signal corresponding thereto.

27. The clock generator circuit of claim 26 wherein the first delay-lock loop delay locks the first clock signal and the last clock signal to each other so that the first clock signal and the last clock signal have a predetermined phase with respect to each other.

28. The command data latch circuit of claim 27 wherein the first clock signal and the last clock signal are delay locked to each other so that they are the inverse of each other.

29. The command data latch circuit of claim 26 wherein the clock signals in the sequence are increasingly delayed in equal increments from the first clock signal to the last clock signal so that adjacent clock signals in the sequence have respective phases that are equally spaced from each other.

30. The command data latch circuit of claim 26 wherein the first delay lock loop delay locks the first clock signal and the last clock signal so that they are the inverse of each other whereby the first and last clock signals have respective phases that are 180 degrees from each other.

31. The command data latch circuit of claim 26 wherein the second delay-lock loop delay locks the first clock signals to the master clock signal so that they have substantially the same phase.

32. The command data latch circuit of claim 26 wherein the first delay-locked loop comprises:

a first voltage controlled delay circuit receiving a reference clock signal and generating the sequence of clock signals from the reference clock signal by delaying the reference clock signal by respective delays that are a function of a first control signal;

a first phase detector comparing the phase of two of the clock signals in the sequence and generating the first control signal as a function of the difference therebetween; and

wherein the second delay-locked loop comprises:

a second voltage controlled delay circuit receiving the master clock signal and generating a reference clock signal having a delay relative to the master clock signal that is a function of a second control signal; and

a second phase detector comparing the phase of the master clock signal to the phase of one of the clock signals in the sequence and generating the second control signal as a function of the difference therebetween.

33. The command data latch circuit of claim 32 wherein each of the first and second phase detectors comprise:

a phase comparator generating a first signal during the period that the phase of the signal applied to one of its input terminals lags the phase of the signal applied to the other of its input terminals and generating a second signal during the period that the phase of the signal applied to the one input terminal leads the phase of the signal applied to the other input terminal; and

a charge pump receiving the first and second signals from the phase comparator, the charge pump generating as the respective first and second control signal a voltage that increases toward one polarity responsive to the first signal and toward the opposite polarity responsive to the second signal.

34. The command data latch circuit of claim 26, further comprising a multiplexer coupled to the first delay-lock loop to receive the clock signals and couple one of the clock signals to a clock output terminal.

35. A packetized dynamic random access memory, comprising:

at least one array of memory cells adapted to store data at a location determined by a row address and a column address responsive to a command word;

a row address circuit adapted to receive and decode the row address, and select a row of memory cells corresponding to the row address responsive to the command word;

a column address circuit adapted to receive or apply data to one of the memory cells in the selected row corresponding to the column address responsive to the command word;

a data path circuit adapted to couple data between an external terminal and the column address circuit responsive to the command word; and

a command data latch circuit for storing a command data packet at a time determined from a command clock signal, the command data latch comprising:

a latch circuit having a data input and a clock input, the data input being adapted to receive the command data packet and store the command data packet responsive to a clock signal applied to the clock input; and

a clock generator circuit for generating the latch signal from a master clock signal, the clock generator circuit comprising:

a first delay-lock loop generating a sequence of clock signals which are increasingly delayed from a first clock signal to a last clock signal, two of the clock signals in the sequence being delay locked to each other so that they have a predetermined phase with respect to each other; and

a second delay-lock loop delay locking one of the clock signals to the master clock signal so that the clock signals in the sequence have respective phases with respect to the master clock signal;

a multiplexer coupled to the first delay-lock loop to receive the clock signals and couple one of the clock signals to the clock input of the latch circuit, the clock signal coupled to the latch circuit being selected by the multiplexer as a function of a select signal applied to a control input of the multiplexer; and

a select circuit determining which of the clock signals from the first delay-lock loop should be used to cause the latch circuit to store the

command data packet and generating the select signal corresponding thereto.

36. The packetized dynamic random access memory of claim 35 wherein the first delay-lock loop delay locks the first clock signal and the last clock signal to each other so that the first clock signal and the last clock signal have a predetermined phase with respect to each other.

37. The packetized dynamic random access memory of claim 36 wherein the first clock signal and the last clock signal are delay locked to each other so that they are the inverse of each other.

38. The packetized dynamic random access memory of claim 35 wherein the clock signals in the sequence are increasingly delayed in equal increments from the first clock signal to the last clock signal so that adjacent clock signals in the sequence have respective phases that are equally spaced from each other.

39. The packetized dynamic random access memory of claim 35 wherein the first delay lock loop delay locks the first clock signal and the last clock signal so that they are the inverse of each other whereby the first and last clock signals have respective phases that are 180 degrees from each other.

40. The packetized dynamic random access memory of claim 35 wherein the second delay-lock loop delay locks the first clock signals to the master clock signal so that they have substantially the same phase.

41. The packetized dynamic random access memory of claim 35 wherein the first delay-locked loop comprises:

a first voltage controlled delay circuit receiving a reference clock signal and generating the sequence of clock signals from the reference clock signal by delaying the reference clock signal by respective delays that are a function of a first control signal;

a first phase detector comparing the phase of two of the clock signals in the sequence and generating the first control signal as a function of the difference therebetween; and

wherein the second delay-locked loop comprises:

a second voltage controlled delay circuit receiving the master clock signal and generating a reference clock signal having a delay relative to the master clock signal that is a function of a second control signal; and

a second phase detector comparing the phase of the master clock signal to the phase of one of the clock signals in the sequence and generating the second control signal as a function of the difference therebetween.

42. A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system; and

a memory coupled to the processor bus adapted to allow data to be stored, the dynamic random access memory comprising:

at least one array of memory cells adapted to store data at a location determined by a row address and a column address responsive to a command word;

a row address circuit adapted to receive and decode the row address, and select a row of memory cells corresponding to the row address responsive to the command word;

a column address circuit adapted to receive or apply data to one of the memory cells in the selected row corresponding to the column address responsive to the command word;

a data path circuit adapted to couple data between an external terminal and the column address circuit responsive to the command word; and

a command data latch circuit for storing a command data packet at a time determined from a command clock signal, the command data latch comprising:

a latch circuit having a data input and a clock input, the data input being adapted to receive the command data packet and store the command data packet responsive to a clock signal applied to the clock input; and

a clock generator circuit for generating the latch signal from a master clock signal, the clock generator circuit comprising:

a first delay-lock loop generating a sequence of clock signals which are increasingly delayed from a first clock signal to a last clock signal, two of the clock signals in the sequence being delay locked to each other so that they have a predetermined phase with respect to each other; and

a second delay-lock loop delay locking one of the clock signals to the master clock signal so that the clock signals in the sequence have respective phases with respect to the master clock signal;

a multiplexer coupled to the first delay-lock loop to receive the clock signals and couple one of the clock signals to

the clock input of the latch circuit, the clock signal coupled to the latch circuit being selected by the multiplexer as a function of a select signal applied to a control input of the multiplexer; and

a select circuit determining which of the clock signals from the first delay-lock loop should be used to cause the latch circuit to store the command data packet and generating the select signal corresponding thereto.

43. The computer system of claim 42 wherein the first delay-lock loop delay locks the first clock signal and the last clock signal to each other so that the first clock signal and the last clock signal have a predetermined phase with respect to each other.

44. The computer system of claim 43 wherein the first clock signal and the last clock signal are delay locked to each other so that they are the inverse of each other.

45. The computer system of claim 42 wherein the clock signals in the sequence are increasingly delayed in equal increments from the first clock signal to the last clock signal so that adjacent clock signals in the sequence have respective phases that are equally spaced from each other.

46. The computer system of claim 42 wherein the first delay lock loop delay locks the first clock signal and the last clock signal so that they are the inverse of each other whereby the first and last clock signals have respective phases that are 180 degrees from each other.

47. The computer system of claim 42 wherein the second delay-lock loop delay locks the first clock signals to the master clock signal so that they have substantially the same phase.

48. The computer system of claim 42 wherein the first delay-locked loop comprises:

a first voltage controlled delay circuit receiving a reference clock signal and generating the sequence of clock signals from the reference clock signal by delaying the reference clock signal by respective delays that are a function of a first control signal;

a first phase detector comparing the phase of two of the clock signals in the sequence and generating the first control signal as a function of the difference therebetween; and

wherein the second delay-locked loop comprises:

a second voltage controlled delay circuit receiving the master clock signal and generating a reference clock signal having a delay relative to the master clock signal that is a function of a second control signal; and

a second phase detector comparing the phase of the master clock signal to the phase of one of the clock signals in the sequence and generating the second control signal as a function of the difference therebetween.

49. A method of generating a sequence of clock signals, comprising:

delay locking a reference clock signal to a master clock signal so that the reference clock signal has a predetermined phase relative to the phase of the master clock signal; and

delay locking a plurality of clock signals to the reference clock signal so that the plurality of clock signals have respective phases relative to the phase of the reference clock signal.

50. The method of claim 49 wherein the reference clock signal is locked to the same phase as the master clock signal.

51. The method of claim 50 wherein a first of the plurality of clock signals has the same phase as the master clock signal, a second of the plurality of clock signals has a phase opposite the phase of the reference clock signals, and the remainder of the plurality of clock signals have respective phases that are equally spaced from each other between the phases of the first and second clock signals.

52. A method of generating a sequence of clock signals from a master clock signal, comprising:

generating the sequence of clock signals each of which has a respective phase that increases from a first clock signal to a last clock signal in the sequence;

delay locking the first clock signal and last clock signals to each other so that they have a predetermined phase with respect to each other;

delay locking one of the clock signals to the master clock signal so that each of the clock signals in the sequence have respective phases with respect to the master clock signal.

53. The method of claim 52 wherein the step of delay locking the first clock signal and the last clock signal comprises delay locking the first clock signal and the last clock signal so that they have respective phases that are 180 degrees from each other.

54. The method of claim 52 wherein the step of delay locking one of the clock signals to the master clock signal comprises delay locking the first clock signals to the master clock signal.

55. The method of claim 54 wherein the step of delay locking the first clock signal to the master clock signal comprises delay locking the first clock signal to the master clock signal so that they have substantially the same phase.

56. The method of claim 52 wherein the step of generating the sequence of clock signals comprises generating the sequence of clock signals so that they have respective phases relative to the phase of the master clock that increase uniformly from a first clock signal to a last clock signal in the sequence.